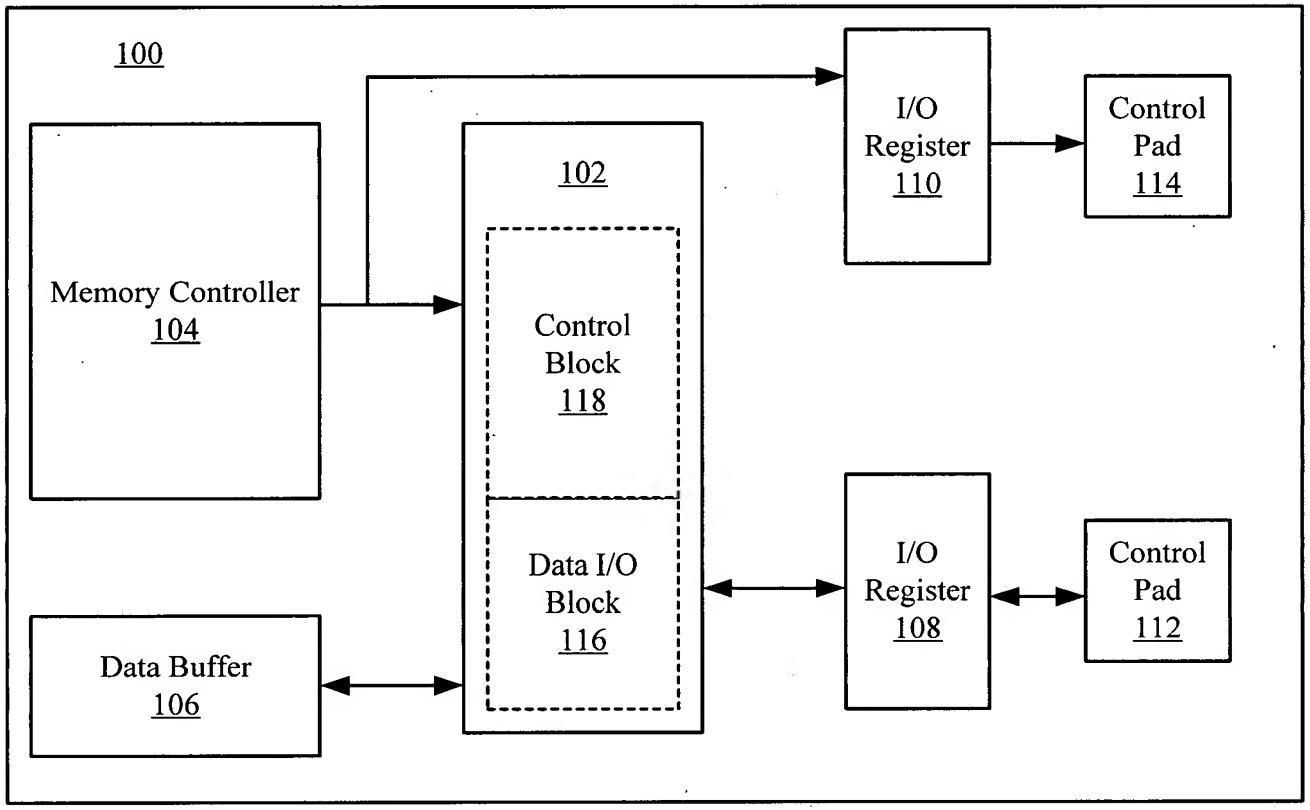
100
Memory Controller
104
Data Buffer
106
102
Control
Block
118
Data I/O
Block
116
I/O
Register
110
Control
Pad
114
I/O
Register
108
Control
Pad
112

FIG. 1

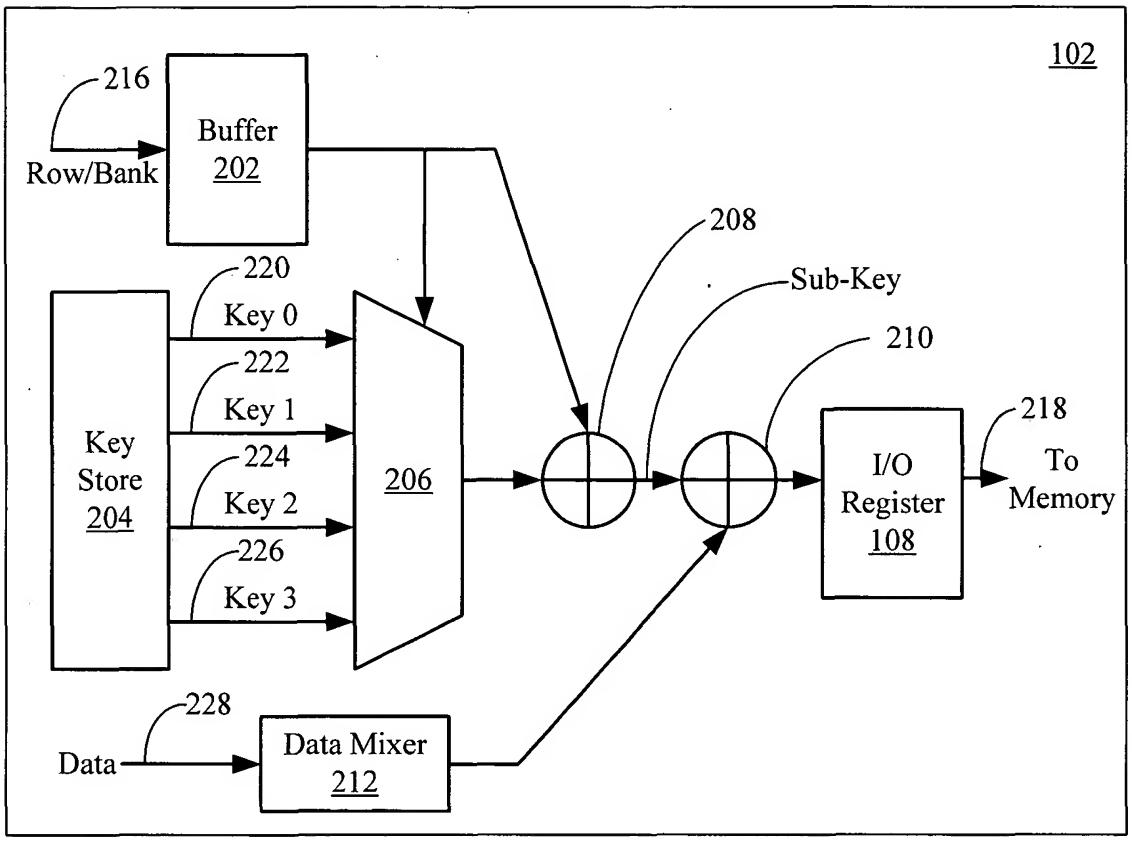
102
216
Row/Bank
Buffer
202
208
Sub-Key
210
220
Key 0
222
Key 1
224
Key 2
226
Key 3
Key
Store
204
206
I/O
Register
108
218
To
Memory
228
Data
Data Mixer
212

FIG. 2

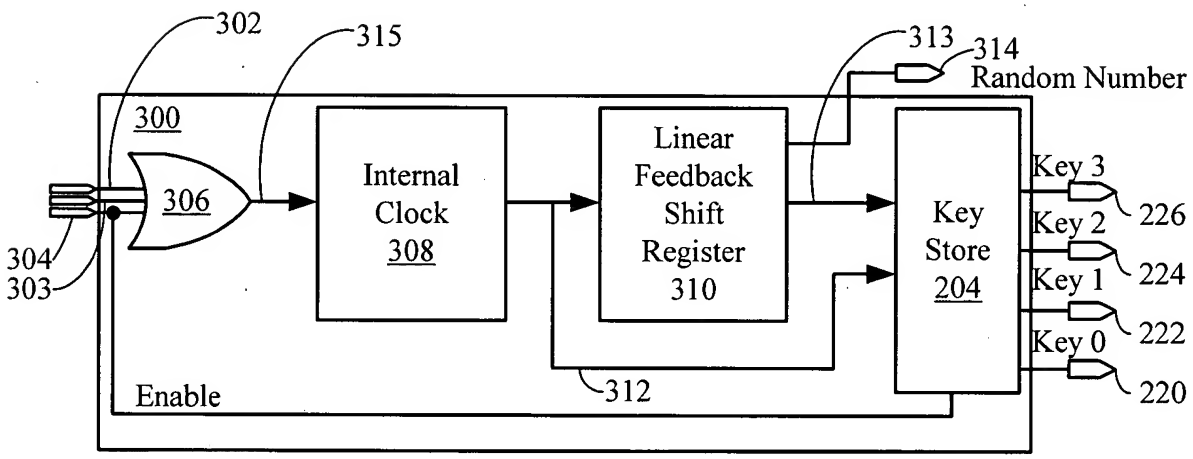
302
315
313
314
Random Number
300
306
Internal
Clock
308
Linear
Feedback
Shift
Register
310
Key
Store
204
Key 3
Key 2
Key 1
Key 0
226
224
222
220
304
303
Enable
312

FIG. 3

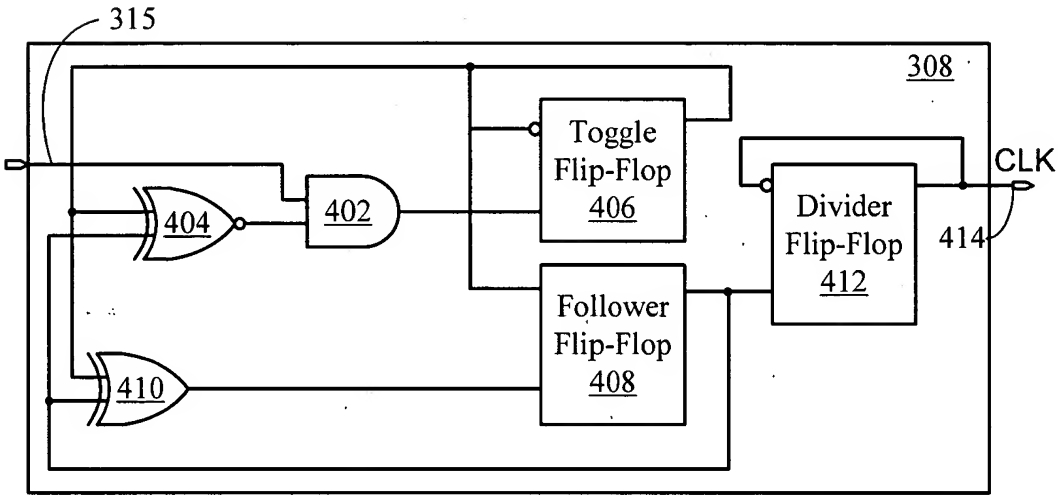
315
308
Toggle
Flip-Flop
406
Divider
Flip-Flop
412
CLK
414
404
402
Follower
Flip-Flop
408
410

FIG. 4

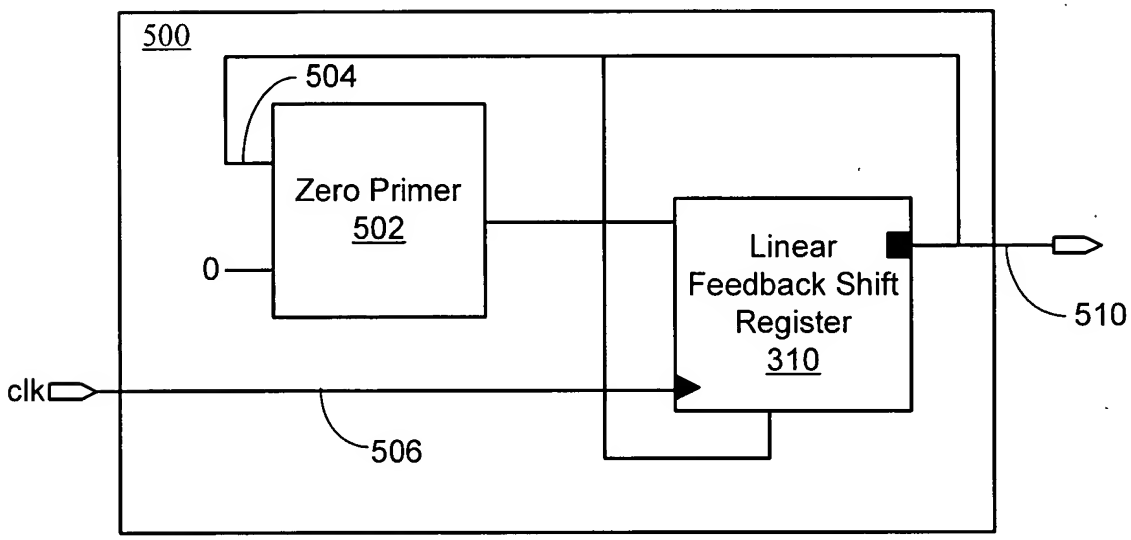
500
504
Zero Primer
502
0
Linear
Feedback Shift
Register
310
510
clk
506

FIG. 5

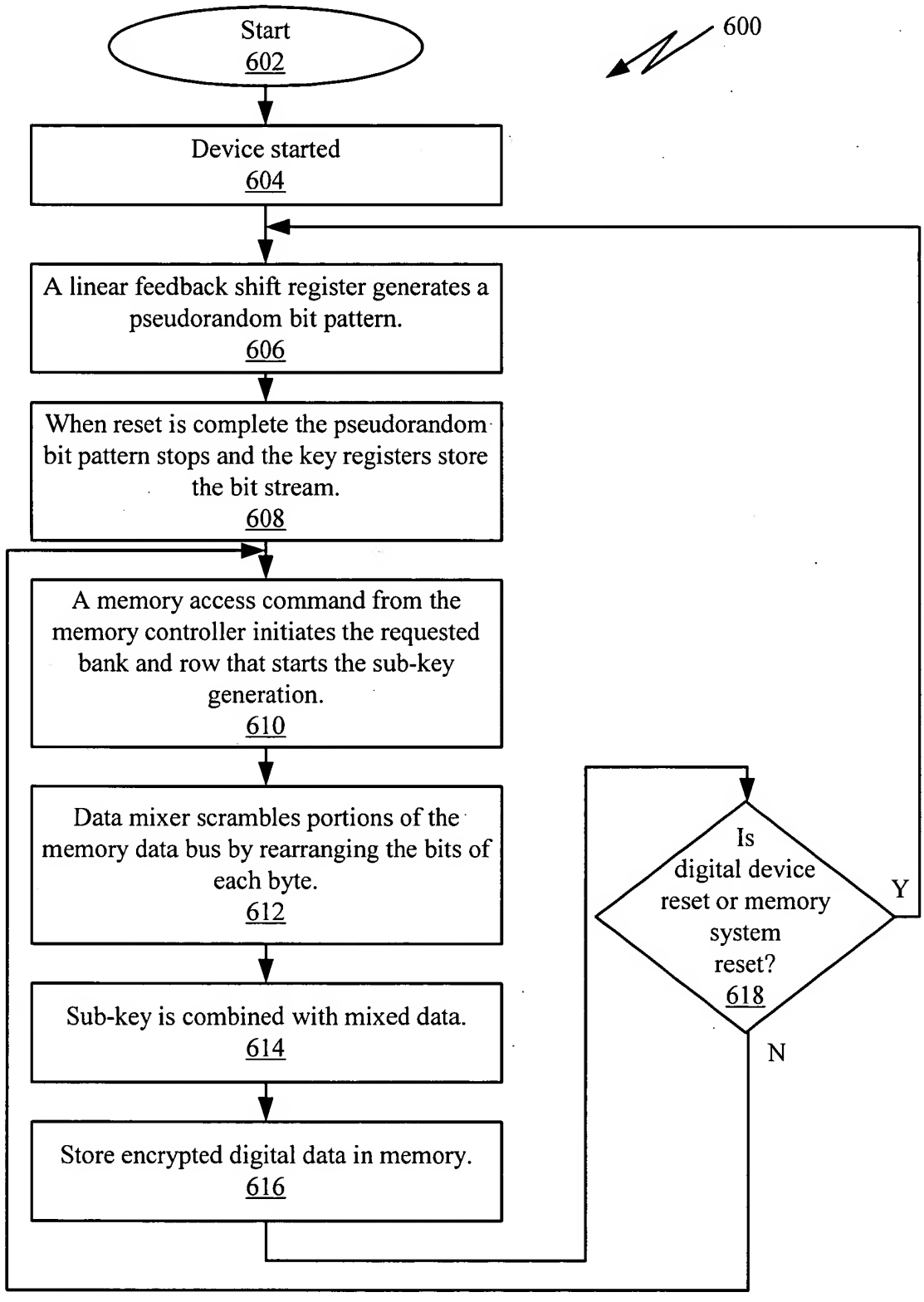
600
Start
602
Device started
604
A linear feedback shift register generates a pseudorandom bit pattern.
606
When reset is complete the pseudorandom bit pattern stops and the key registers store the bit stream.
608
A memory access command from the memory controller initiates the requested bank and row that starts the sub-key generation.
610
Data mixer scrambles portions of the memory data bus by rearranging the bits of each byte.
612
Sub-key is combined with mixed data.
614
Store encrypted digital data in memory.
616
Is digital device reset or memory system reset?
618
Y
N

FIG. 6

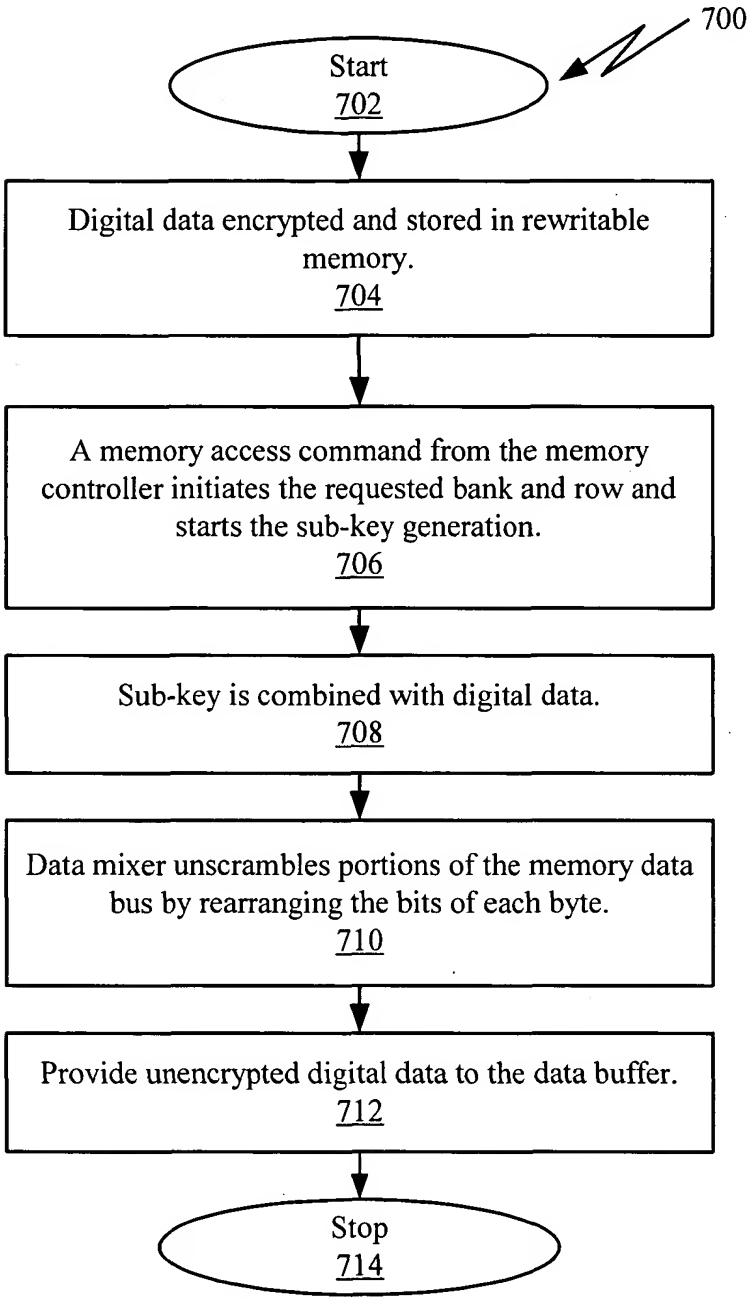
700
Start
702
Digital data encrypted and stored in rewritable memory.
704
A memory access command from the memory controller initiates the requested bank and row and starts the sub-key generation.
706
Sub-key is combined with digital data.
708
Data mixer unscrambles portions of the memory data bus by rearranging the bits of each byte.
710
Provide unencrypted digital data to the data buffer.
712
Stop
714

FIG. 7